

Signal-Stage PFC Buck Current Control LED Driver

DESCRIPTION

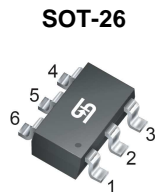
The TS19720 is a high power factor and high accuracy constant current PWM controller. It is able to control total harmonic distortion (THD) and efficiency optimization by an external resistor. TS19720 achieves high power factor and high efficiency by boundary conduction mode (BCM). The line and load regulation of LED current are within $\pm 2.5\%$. TS19720 also provides gate driving voltage clamping, V_{CC} over-voltage protection, and system output open/short circuit protection to increase IC performance.

FEATURES

- Low THD <15%
- Constant Current Accuracy within $\pm 2.5\%$
- High Power Factor >0.9
- Low BOM Cost
- Boundary Conduction Mode Control
- Gate Output Voltage Clamp
- LED Open Protection
- LED Short Protection
- Over Current Protection (OCP)
- Over Thermal Protection (OTP)

APPLICATION

- LED lighting
- Down light
- Tube lamp
- PAR lamp
- Bulb

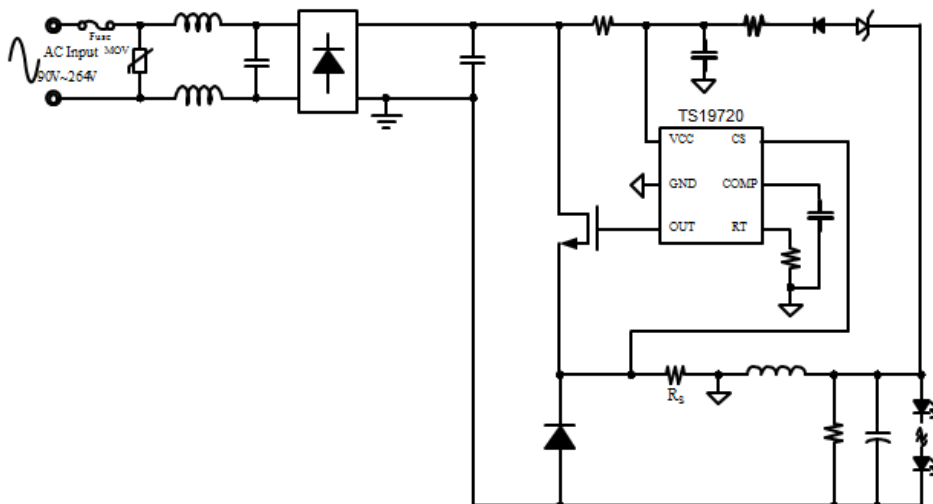


Pin Definition:

1. V_{CC}
2. GND
3. OUT
4. RT
5. COM
6. CS

Notes: Moisture sensitivity level: level 3. Per J-STD-020

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Note 1)			
PARAMETER	SYMBOL	LIMIT	UNIT
Power Supply Pin	V_{CC}	40	V
RT Voltage to GND	V_{RT}	-0.3 to 5.5	V
OUT Voltage to GND	V_{OUT}	-0.3 to 40	V
CS Voltage to GND	V_{CS}	-0.3 to 5.5	V
COM Voltage to GND	V_{COM}	-0.3 to 5.5	V
Power Dissipation @ $T_A=25\text{ }^\circ\text{C}$	P_D	0.3	W
ESD Rating (Human Body Mode) (Note 2)	HBM	2	kV
ESD Rating (Machine Mode)	MM	200	V
Lead Temperature (Soldering 10 sec)	T_{LEAD}	260	$^\circ\text{C}$
Junction Temperature Range	T_J	-40 to +150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-65 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	106.6	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	220	$^\circ\text{C/W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air. Thermal Resistance is specified with the component mounted on a low effective thermal conductivity test board in free air at $T_A=25\text{ }^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS (Note 3)			
PARAMETER	SYMBOL	CONDITIONS	UNIT
Power Supply Pin	V_{CC}	33	V
RT Voltage to GND	V_{RT}	-0.3 to 5	V
OUT Voltage to GND	V_{OUT}	-0.3 to 19	V
CS Voltage to GND	V_{CS}	-0.3 to 5	V
COM Voltage to GND	V_{COM}	-0.3 to 5	V
Operating Junction Temperature Range	T_J	-40 to +125	$^\circ\text{C}$
Operating Ambient Temperature Range	T_{OPA}	-40 to +85	$^\circ\text{C}$

ELECTRICAL SPECIFICATIONS ($V_{CC} = 18V, T_A = 25^{\circ}C$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage						
Start-up Current	$V_{CC} = V_{UVLO(on)} - 1V$	$V_{CC(ST)}$	--	45	--	μA
Operating Current	With 1nF load on out pin	I_{OPA}	--	2.1	2.6	mA
UVLO(off)		$V_{UVLO(off)}$	7	8	9	V
UVLO(on)		$V_{UVLO(on)}$	16	17.5	19	V
OVP Level on V_{CC} Pin		V_{OVP}	29	31	33	V
Voltage Feedback						
Feedback Reference Voltage		V_{FB}	0.196	0.2	0.204	V
Transconductance		G_M	--	58	--	μS
Output Sink Current		I_{O-SINK}	--	5.8	--	μA
Output Source Current		$I_{O-SOURCE}$	--	5.8	--	μA
Current Sensing						
CS Limit Voltage		V_{OCP}	--	1.4	--	V
Open Loop Voltage	CS Pin Open	V_{OLP}	--	5	--	V
Leading-Edge Blanking Time		LEB_t	--	400	--	ns
Delay to Output			--	100	--	ns
Switching Frequency						
Start Frequency		F_{STR}	3	4.5	6	kHz
Gate Driver Output						
Rising Time	Load Capacitance = 1nF	t_{RISE}	--	90	--	ns
Falling Time	Load Capacitance = 1nF	t_{FALL}	--	40	--	ns
VGATE-Clamp		V_{GATE}	--	12.5	15	V
Thermal Section						
Thermal Shutdown ^(Note 4)			--	150	--	$^{\circ}C$
Thermal Shutdown Release ^(Note 5)			--	120	--	$^{\circ}C$

Note:

1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
2. Devices are ESD sensitive. Handling precaution recommended..
3. The device is not guaranteed to function outside its operating conditions.
4. Guaranteed by design.
5. Auto Recovery Type.

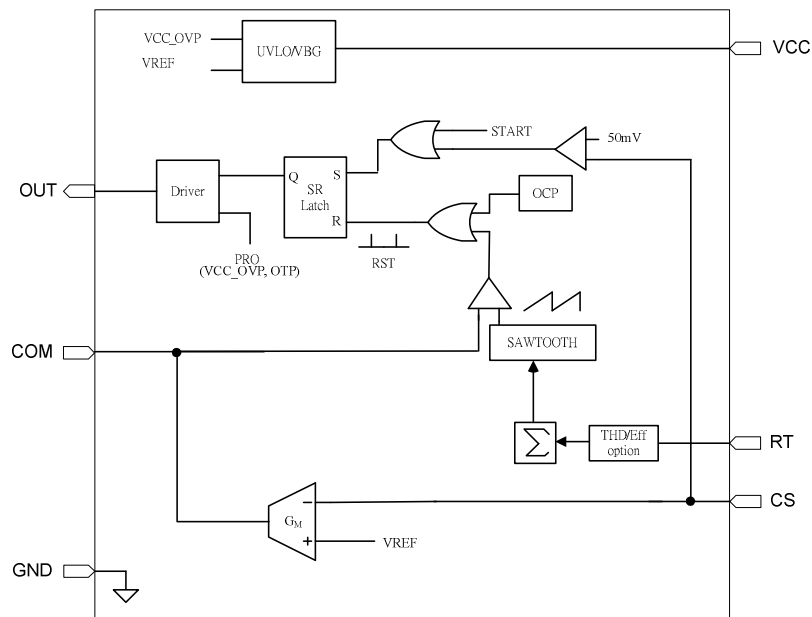
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TS19720CX6 RFG	SOT-26	3,000pcs / 7" Reel

Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC.
2. Halogen-free according to IEC 61249-2-21 definition.

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V _{CC}	Power supply pin for all internal circuitry
2	GND	Ground return for all internal circuitry
3	OUT	Gate driver output
4	RT	Efficiency / THD option pin
5	COM	Output pin of error amplifier
6	CS	Input current sense pin

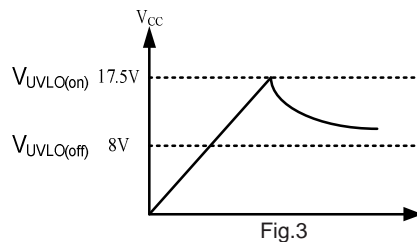
APPLICATION INFORMATION

Start-up Current

The typical start-up current is around 45μA. Very low start-up current allows the PWM controller to increase the value of start-up resistor and then reduce the power dissipation.

Under Voltage Lockout (UVLO)

A hysteresis UVLO comparator is implemented in TS19720. The turn-on and turn-off thresholds level are fixed at 17.5V and 8V respectively. This hysteresis shown in Fig.3 ensures that the start-up capacitor will be adequate to supply the chip during start-up. For quick start-up of the LED driver, the start-up resistor should be matched with the start-up capacitor.



Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense resistor. To avoid fault trigger, a 400ns leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Gate Clamp

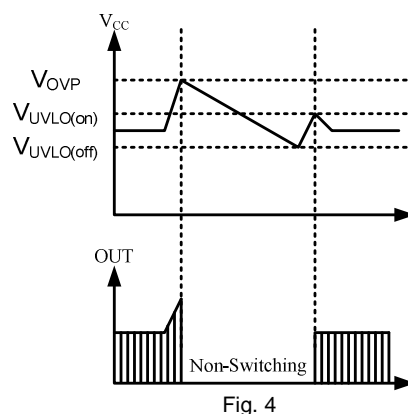
Driver is clamped to 12.5V by an internal clamping circuit to avoid the Gate of MOSFET to get damaged.

Over Current Protection (OCP)

The TS19720 has built-in cycle by cycle over current protection function on CS pin. As the CS pin voltage is larger than V_{OCP} (1.4V), the gate output will be turned off immediately to avoid the driver board to be burned out.

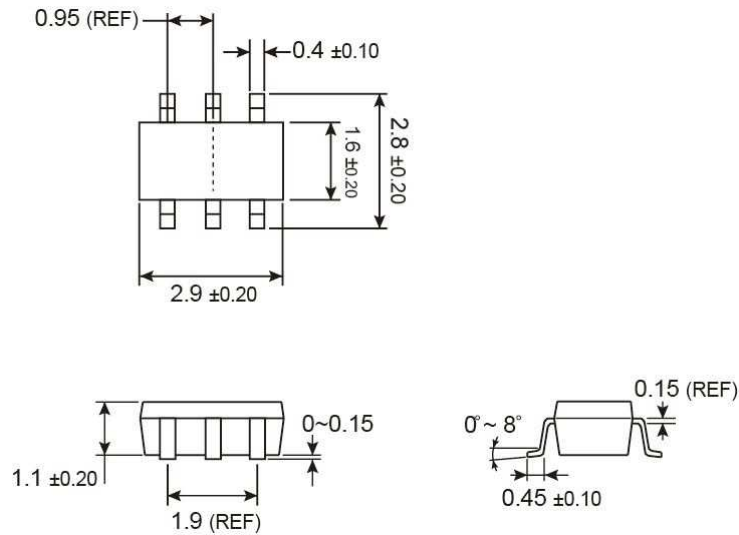
Over Voltage Protection (OVP) on V_{CC}

To prevent the LED driver from being damaged, the TS19720 has an implemented OVP function on V_{CC}. When the V_{CC} voltage is higher than the V_{OVP} (31V), the output gate driver circuit will be shut down immediately to stop the switching of power MOSFET. The V_{CC} pin OVP function is an auto recovery type protection. If the OVP condition happens, the pulses will be stopped until the V_{CC} pin voltage is down to the UVLO off level. The TS19720 is working in an auto-recovery mode as shown in Fig. 4.

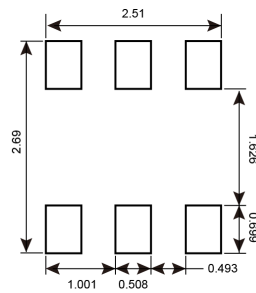


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

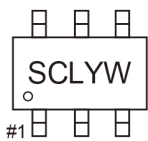
SOT-26



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- SC** = Device Code
- Y** = Year Code
 - D** =2014 **E** =2015 **F** =2016 **G** =2017
 - H** =2018 **J** =2019 **K** =2020
- W** = Week Code
 - A~Z** =wk1~wk26
 - A~Z** = wk27~wk52
- L** = Lot Code A~Z

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